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Terms	Documents
L5 and (logic near2 circuits)	3

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
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Search: L6

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DATE: Friday, September 27, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L6	L5 and (logic near2 circuits)	3	L6
L5	L4 and (silicon adj oxide) and (silicon adj nitride)	17	L5
L4	L2 and (bit adj lines) and (insulat$)	75	L4
L3	L2 and (fourth near2 insulat$)	9	L3
L2	L1 and (fourth near2 (word adj lines))	166	L2
L1	DRAM	32867	L1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 6312982 B1

L6: Entry 1 of 3 File: USPT Nov 6, 2001

US-PAT-NO: 6312982
DOCUMENT-IDENTIFIER: US 6312982 B1

TITLE: Method of fabricating a trench capacitor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Draw. Desc | Image KWIC

☐ 2. Document ID: US 6235620 B1

L6: Entry 2 of 3 File: USPT May 22, 2001

US-PAT-NO: 6235620
DOCUMENT-IDENTIFIER: US 6235620 B1

TITLE: Process for manufacturing semiconductor integrated circuit device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Draw. Desc | Image KWIC

☐ 3. Document ID: US 5188975 A

L6: Entry 3 of 3 File: USPT Feb 23, 1993

US-PAT-NO: 5188975
DOCUMENT-IDENTIFIER: US 5188975 A

TITLE: Method of producing a connection hole for a DRAM having at least three conductor layers in a self alignment manner.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Draw. Desc | Image KWIC

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Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 6309930 B1

L3: Entry 1 of 9 File: USPT Oct 30, 2001

US-PAT-NO: 6309930
DOCUMENT-IDENTIFIER: US 6309930 B1

TITLE: SRAM cell arrangement and method for manufacturing same

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 6235620 B1

L3: Entry 2 of 9 File: USPT May 22, 2001

US-PAT-NO: 6235620
DOCUMENT-IDENTIFIER: US 6235620 B1

TITLE: Process for manufacturing semiconductor integrated circuit device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 3. Document ID: US 5899734 A

L3: Entry 3 of 9 File: USPT May 4, 1999

US-PAT-NO: 5899734
DOCUMENT-IDENTIFIER: US 5899734 A

TITLE: Method of fabricating semiconductor device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

☐ 4. Document ID: US 5875148 A

L3: Entry 4 of 9 File: USPT Feb 23, 1999

US-PAT-NO: 5875148
DOCUMENT-IDENTIFIER: US 5875148 A

TITLE: Semiconductor memory

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 5. Document ID: US 5296402 A

L3: Entry 5 of 9 File: USPT Mar 22, 1994

US-PAT-NO: 5296402
DOCUMENT-IDENTIFIER: US 5296402 A

TITLE: Method for manufacturing a DRAM having a second effective capacitor area

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 6. Document ID: US 5188975 A

L3: Entry 6 of 9 File: USPT Feb 23, 1993

US-PAT-NO: 5188975
DOCUMENT-IDENTIFIER: US 5188975 A

TITLE: Method of producing a connection hole for a DRAM having at least three conductor layers in a self alignment manner.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 7. Document ID: US 5034341 A

L3: Entry 7 of 9 File: USPT Jul 23, 1991

US-PAT-NO: 5034341
DOCUMENT-IDENTIFIER: US 5034341 A

TITLE: Method of making a memory cell array structure

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 8. Document ID: US 4920389 A

L3: Entry 8 of 9 File: USPT Apr 24, 1990

US-PAT-NO: 4920389
DOCUMENT-IDENTIFIER: US 4920389 A

TITLE: Memory call array structure and process for producing the same

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Drawi Desc | Image

☐ 9. Document ID: US 4912535 A

L3: Entry 9 of 9 File: USPT Mar 27, 1990

US-PAT-NO: 4912535
DOCUMENT-IDENTIFIER: US 4912535 A

TITLE: Trench type semiconductor memory device having side wall contact

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Drawi Desc | Image

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Terms	Documents
L2 and (fourth near2 insulat$)	9

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L3: Entry 1 of 9 File: USPT Oct 30, 2001

DOCUMENT-IDENTIFIER: US 6309930 B1
TITLE: SRAM cell arrangement and method for manufacturing same

Brief Summary Text (5):
An SRAM cell arrangement is a memory cell arrangement with random access to stored information. In contrast to a DRAM cell arrangement wherein the information must be refreshed at regular time intervals, the information is statically stored in an SRAM cell arrangement.

Drawing Description Text (7):
FIG. 6A shows the cross-section from FIG. 5 after a fourth insulating structure, first contacts, third contacts, seventh contacts, eighth contacts, fourth conductive structures, first bit lines and second bit lines were produced;

Detailed Description Text (40):
Borophosphorous glass is deposited in a thickness of approximately 600 nm. The borophosphorous glass is planarized with the assistance of chemical-mechanical polishing. As a result, a fourth insulating structure 14 arises (see FIG. 6A). For producing first contacts KI that contact the second source/drain regions I S/D2 of the first transistors, third contacts that contact the first source/drain regions 3 S/DI of the third transistors, seventh contacts K7 that contact the second source/drain regions S/D2 of the fifth transistors, and eighth contacts that contact the second source/drain regions 6 S/D2 of the sixth transistors, borophosphorous glass is etched selectively, relative to silicon, with the assistance of a seventeenth mask (not shown) of photoresist until parts of the source/drain regions are uncovered. C.sub.2 F.sub.6 +O.sub.2, for example, is suitable as an etchant.

Other Reference Publication (3):
"High-Density Thin Film Transistor Load SRAM Cell Using Trench DRAM Technology," IBM Technical Disclosure Bulletin, vol. 36, No. 09A, Sep. 1993, pp. 581-582.

CLAIMS:

1. A method for manufacturing an SRAM cell arrangement which includes a plurality of memory cells, wherein the manufacture of each memory cell respectively comprises the steps of:

forming first, second, third, fourth, fifth and sixth vertical MOS transistors, wherein each transistor includes a gate electrode, a

first source/drain region and a second source/drain region, and wherein the third and fourth transistors are complementary to the first, second, fifth and sixth transistors;

forming a word line, first bit line and second bit line, wherein the first bit line is formed transversely relative to the word line and the second bit line is formed parallel to the first bit line;

connecting the first source/drain region of the first transistor to both the first source/drain region of the second transistor and a first voltage terminal;

connecting the second source/drain region of the first transistor to each of the first source/drain region of the first transistor, the first source/drain region of the fifth transistor, the gate electrode of the second transistor and the gate electrode of the fourth transistor;

connecting the gate electrode of the first transistor to each of the second source/drain region of the second transistor, the first source/drain region of the fourth transistor, the gate electrode of the third transistor and the first source/drain region of the sixth transistor;

connecting the second source/drain region of the third transistor to each of the second source/drain region of the fourth transistor and the a second voltage terminal;

connecting the second source/drain region of the fifth transistor to the first bit line;

connecting the gate electrode of the fifth transistor to both the gate electrode of the sixth transistor and the word line;

connecting the second source/drain region of the sixth transistor to the second bit line;

forming first, second and fourth trenches in a substrate, wherein the first, second and fourth trenches are substantially parallel to each other, wherein the first and second transistors are adjacent a second side wall of the first trench wherein the fifth and sixth transistors are adjacent a second side wall of the second trench, wherein the third and fourth transistors are adjacent a first side wall of the fourth trench, and wherein the word line is arranged along the second side wall of the second trench;

providing the side walls of each of the first, second and fourth trenches with a gate dielectric;

forming a first conductive structure that is connected to the first voltage terminal along the first trench;

forming a second conductive structure that is connected to the second voltage terminal along the fourth trench;

connecting both the first source/drain region of the first transistor and the first source/drain region of the second